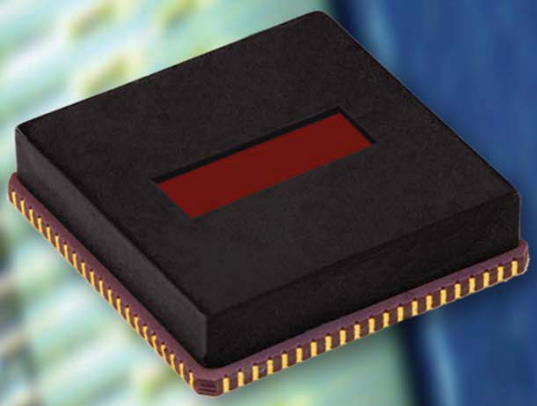
Infrared Materials

The Leader in High Performance IR Detectors

PbSe

256 Pixel MWIR Linear Array

1.2 to 5.5 Microns



Integral TEC | -20°C Operation (45 Degrees DT)

256 Channel Multiplexer (MUX)

WWW.INFRAREDMATERIALS.COM

707-620-0160

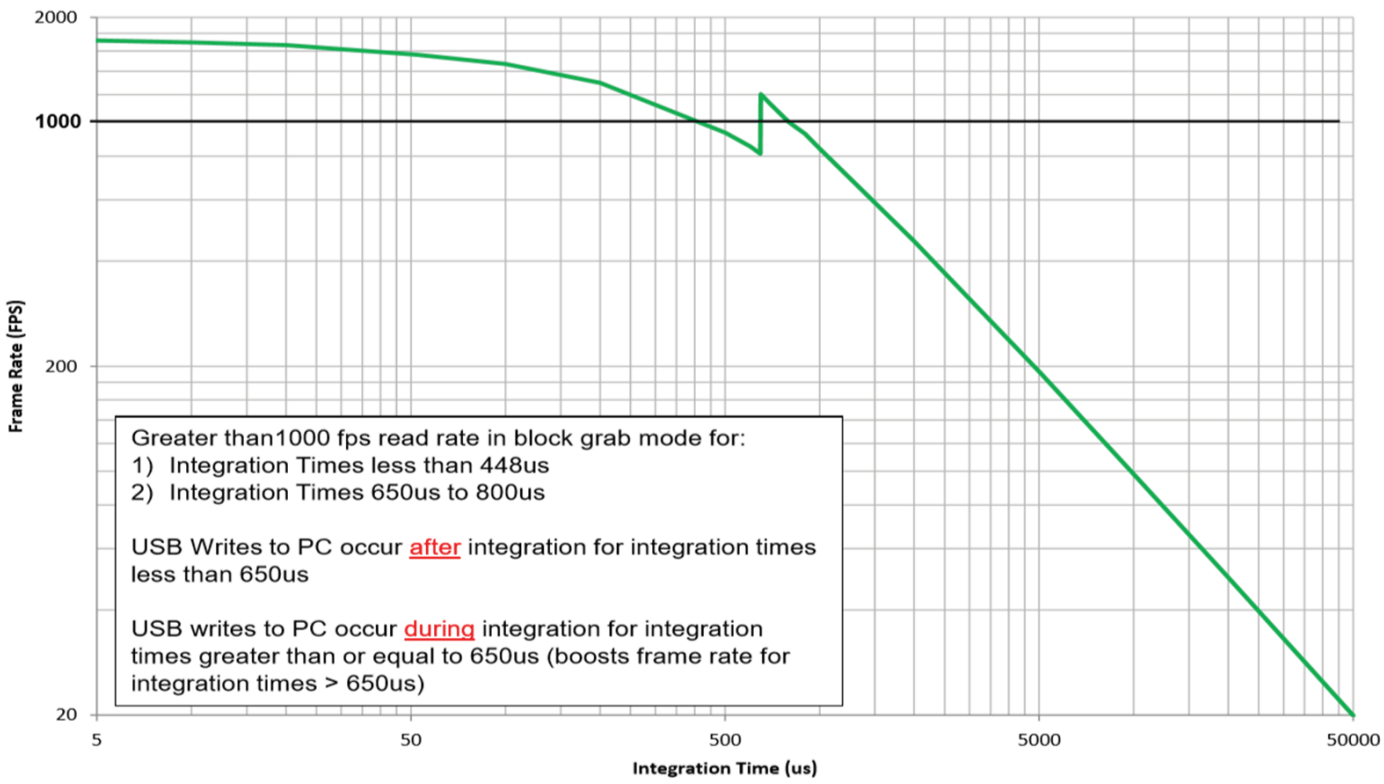
REACH COMPLIANT

RoHS COMPLIANT

PbSe MWIR PHOTOCONDUCTIVE IR ARRAYS | 1.2 - 5.5 MICRONS

Array Mechanical Characteristics				
	Optical Interface	84-pin Leadless Chip Carrier (LCC), 0.317" height, 1.150" Square		
	Window	0.50 mm Thick Silicon with Long Wave Pass (LWP) Anti-Reflective Coating		
	Array Type	PbSe, Lead Selenide, Quantum Photoconductor		
		*PbS versions also available for spectral sensitivity from 1.2 - 3.3 Microns		
	Resolution	256 x 1	--	
	Pixel Size	0.040 x 0.450	--	mm
	Pixel Options	0.040 x 0.040	(Square Pixel)	mm
		0.040 x 4.50	(Long Pixel)	mm
	Array Length	12.85	--	mm
	Pixel Pitch	0.050	(On centers)	mm
	Pixel Operability	> 98%	--	
	Cooling Element	Thermoelectric Cooler (TEC)	1-Stage, 10 Watt, RoHS	5.0 VDC @ 2.0 Amps
	Field of View (FOV)	> 40	--	Degrees
Readout Electronics (ROIC)				
	ADIC PC06 R6 Array Controller	32 Bit microntroller (80 MHz)	16 Bit A/D Converter	On Board EEPROM
	External Hardware Trigger Input	External Shutter Control	Auto Calibration Feature	Integrated TE Cooler Board
	Default Temp range -20 to +25°C	Control Stability to ± 5 mK	Array Software & SDK Available	
	Readout Method	Multiplexer, 256 Channel, DC Integrating w/ Global & 8 Bit Per Pixel Dark Current Correction		
	Readout Control / Windowing	Feature to readout all 256 pixels or a user defined value, e.g., 2, 8, 16, 32, 64, 128, etc.		
	Integration Time Range**	4 (Min.)	--	µs
		210 (Max.)	--	ms
		**Digitally selectable in 3.2 µs steps.		
	Frame Rate***	Sample rates up to 1700 frames per second, 1 to 64K block selectable		
		***Maximum frame rate achieved at the minimum integration time		

Frame Rate vs. Integration Time (Block Grab Mode)



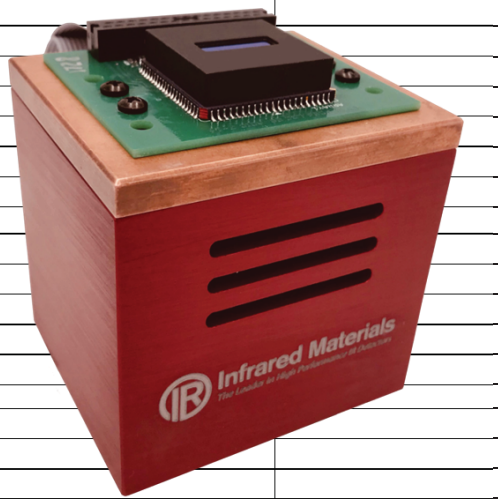
PbSe MWIR PHOTOCONDUCTIVE IR ARRAYS | 1.2 - 5.5 MICRONS

	Operating Modes	Integrate While Read (IWR)		
		Integrate Then Read (ITR)		
	Compatibility	Windows DLL Software Interface, Linux Compatible		
		Programming languages supported: Visual C#, Visual C++, and more.		
	Interface Protocol	USB 2.0 (Ethernet, SPI, RS485 Serial Communication Interfaces Under Development)		
	Power Requirement:			
	Data Acquisition / TEC Controller	15 VDC	1.6 A	--
Spectral Characteristics				
	Operating Range (λ)	1.2**	5.5	Microns
		**Cut-on wavelength is dependent upon the window material		
		Other window options are available for wavelength sensitivity at or below 1.0 Microns.		
	Wavelength Peak (λ_{pk})	>= 4.1 (Min.)	<= 4.3 (Max.)	Microns
Electrical Performance Characteristics				
	Pixel Resistance Range +25°C (Typ.)	10	11	MΩ
	-20°C (Typ.)	50	60	MΩ
	D* (D-Star) Detectivity +25°C	>= 1.8 x 10^{10} (Min.)	No Upper Limit	cm $Hz^{1/2}$ w^{-1}
	Responsivity	2.5 x 10^{5} (min.)	4.0 x 10^{5} (Typ.)	V/W
	Response Uniformity	± 15 of Mean	--	%
	Quantum Efficiency (QE)	2	--	%
	Time Constant (T_c)	2 @ +25°C (Typ.)	20 @ -20°C (Max.)	uSec
	NEP	No Data	--	pW
General Specifications				
	Operating Temperature	-20	--	°C
	Operational Temperature Range	-50	+85	°C
	Maximum Incident Light	1x10^{-3}	--	W/cm2
	Storage Temperature	-50 (Min.)	+85 (Max.)	°C
	Thermistor Resistance	10 ± 5% @ +25°C	Not calibrated	KΩ

PbSe ARRAY DEVELOPMENT SYSTEM (DS)

Development System Kit Includes:

- **256 Element PbSe Array and Headboard**
- **USB Electronic Controller Board R6, Ribbon Cable, USB Cable**
- **Copper Mounting Block**
- **Copper Heatsink with Integrated Fan**
- **System Power Supply Module (12V @ 1A)**
- **Array Controller GUI Software & SDK Library**
- **Users Manual (Also available on website)**



OPERATING MODES:

- **Pixel Stream Output**
- **Spectrometer Mode**
- **Push Broom Imager**

FEATURES:

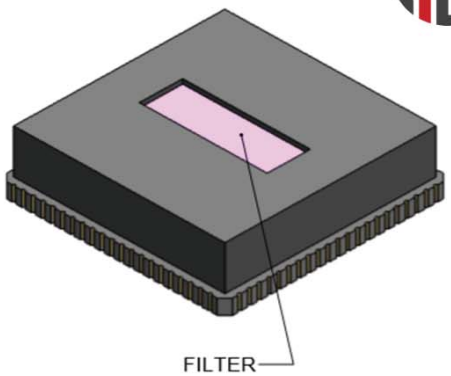
- **External Hardware Trigger Input**
- **External Shutter Control**
- **Auto Calibration Feature**
- **Integrated TE Cooler Board (Control Stability to ± 5 mK)**
- **32 Bit microntroller (80 MHz)**
- **16 Bit A/D Converter**

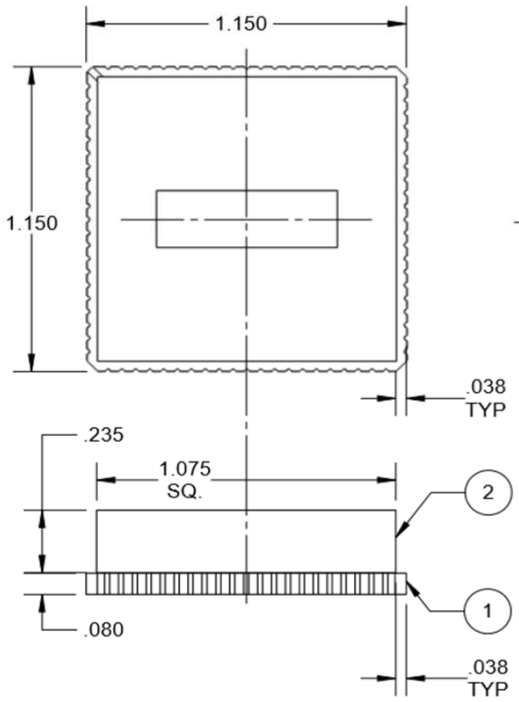
ADDITIONAL DEVELOPMENTS:

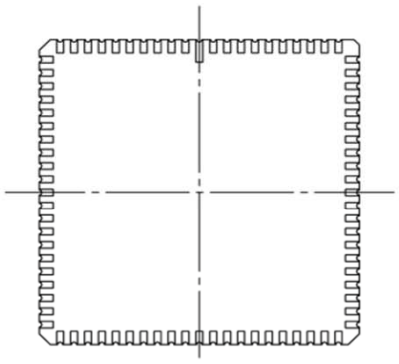
- **Linear Variable Filter (LVF) Integration of PbSe Versions for 2.5 - 5.5 Micron Operating Range**
- **Ethernet Communication Protocol Under Development**

ADDITIONAL TOOLS:

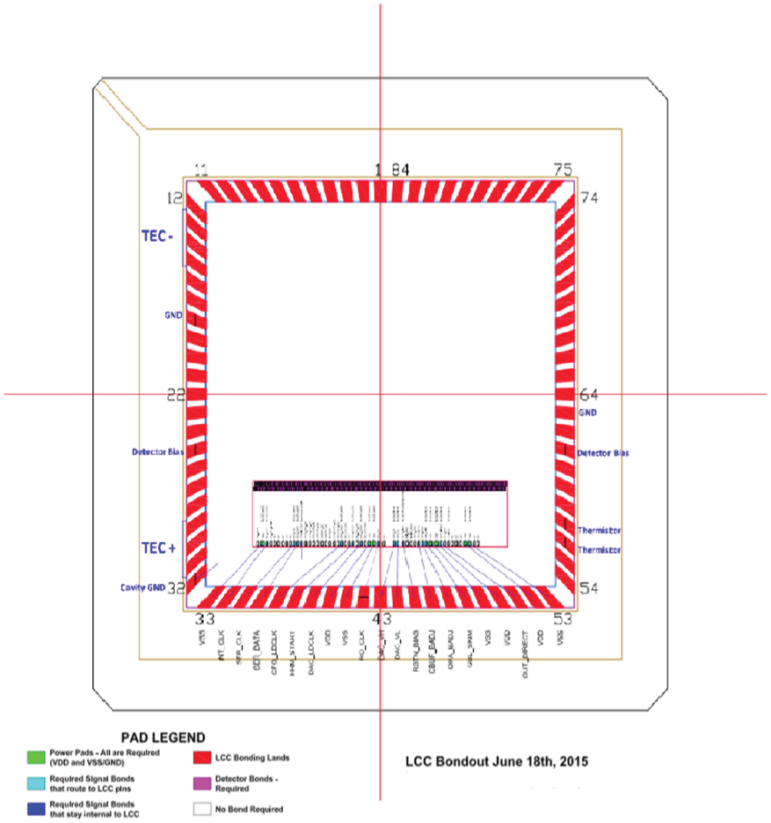
- **3D Model Drawing Available Upon Request for Mechanical Design Considerations**


FILTER

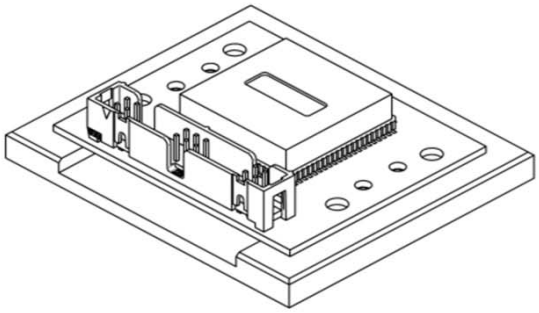

1.150
1.150
.038
TYP
.235
1.075
SQ.
2
1
.080
.038
TYP

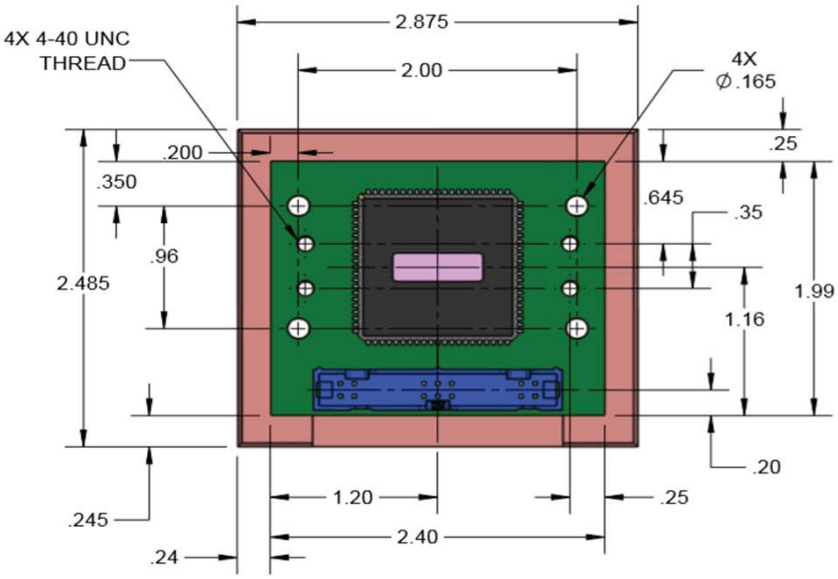


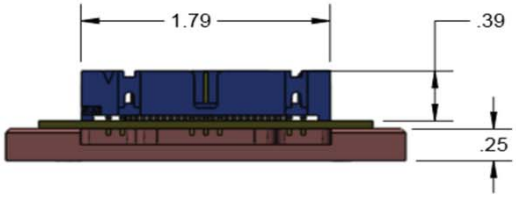
BOTTOM VIEW


1
84
75
12
74
TEC -
GND
22
64
GND
Detector Bias
Detector Bias
Thermistor
Thermistor
TEC +
Cavity GND
32
54
33
43
53
PAD LEGEND
Power Pads - All are Required (VDD and VSS/GND)
Required Signal Bonds that route to LCC pins
Required Signal Bonds that stay internal to LCC
LCC Bonding Lands
Detector Bonds - Required
No Bond Required
LCC Bondout June 18th, 2015

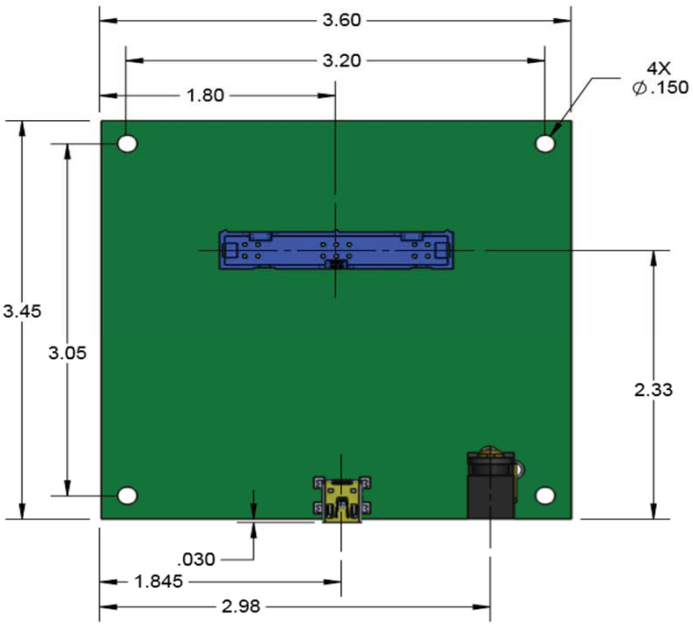
84 LEAD PCB ASSEMBLY

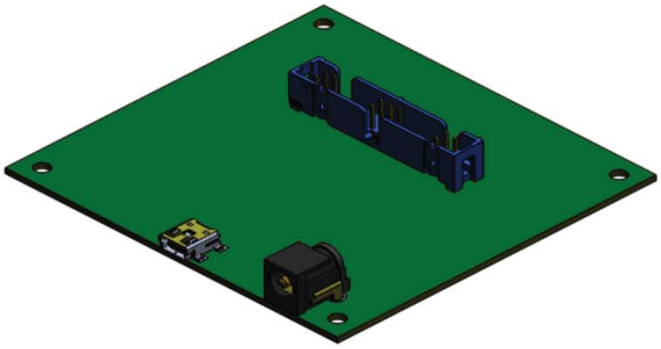


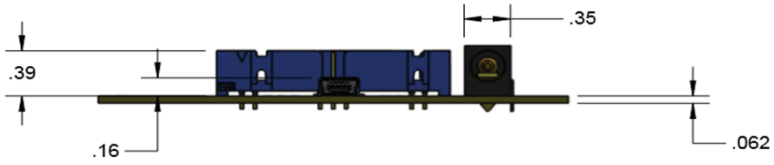


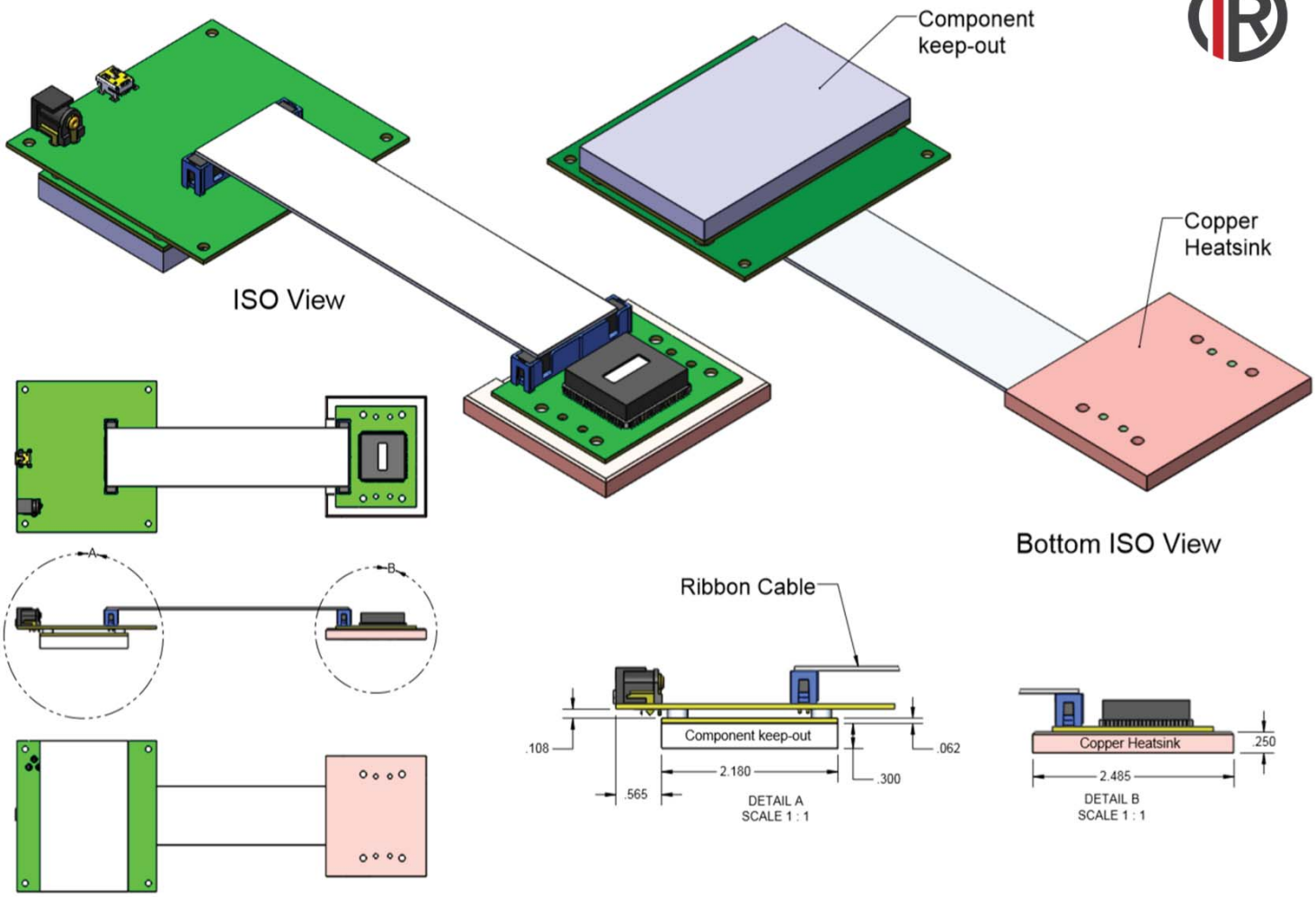


ARRAY R6 ASSEMBLY

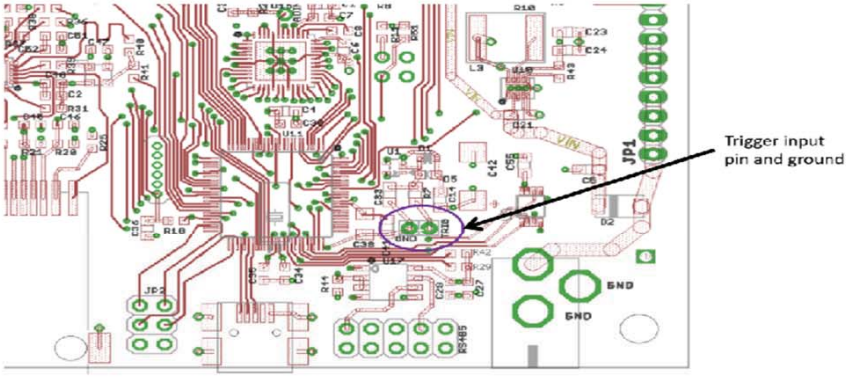


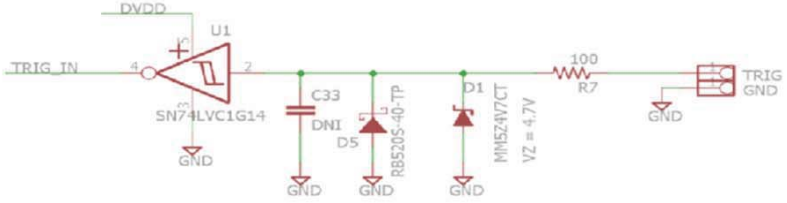




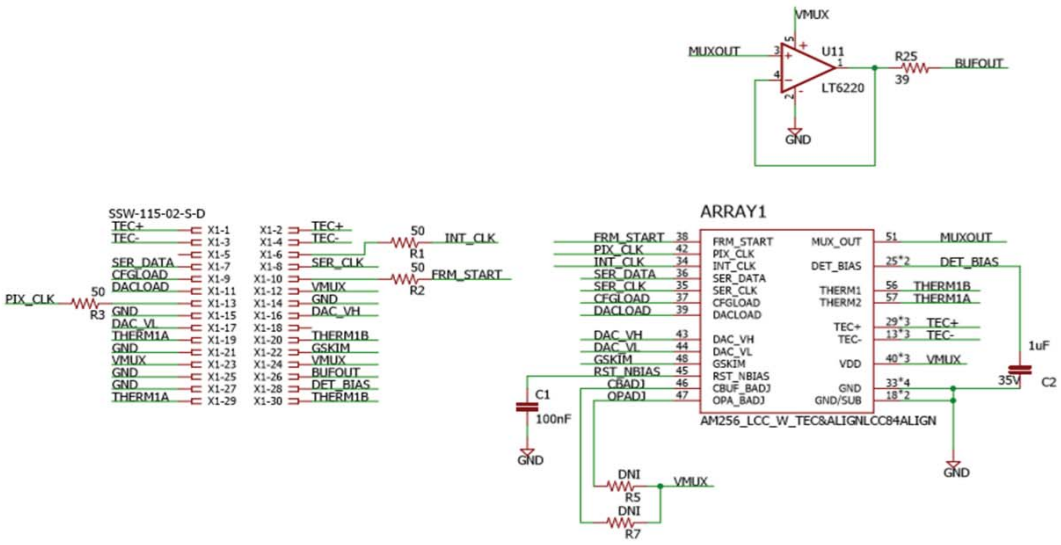


TRIGGER INPUT





INTERFACE BOARD SCHEMATIC - LCC ARRAY



30-PIN CONNECTOR SCHEMATIC

30 Pin Connect Definition			
Signal Name	**Pin**	**Pin**	**Signal Name**
TEC+	**1**	**2**	TEC+
TEC-	**3**	**4**	TEC-
NC	**5**	**6**	INT_CLK
SER_DATA	**7**	**8**	SER_CLK
CFGLOAD	**9**	**10**	FRM_START
DACLOAD	**11**	**12**	VMUX
PIX_CLK	**13**	**14**	GND
GND	**15**	**16**	DAC_VH
DAC_VL	**17**	**18**	NC
THERM_1A	**19**	**20**	THERM_1B
GND	**21**	**22**	GSKIM
VMUX	**23**	**24**	VMUX
GND	**25**	**26**	MUXOUT
GND	**27**	**28**	DET_BIAS
THERM_1A	**29**	**30**	THERM_1B